

APPLICATION  
FOR  
UNITED STATES LETTERS PATENT

TITLE: METHOD FOR MANUFACTURING SEMICONDUCTOR  
DEVICE

APPLICANT: SHIGEHARU MONOE

# METHOD FOR MANUFACTURING SEMICONDUCTOR DEVICE

## BACKGROUND OF THE INVENTION

### 1. Field of the Invention

5           The present invention relates to a method of manufacturing an insulating gate field-effect transistor. In particular, the present invention relates to a method of manufacturing a semiconductor device that can be applied to a thin film transistor (TFT) having a gate overlapping structure.

### 10   2. Related Art

          A display device using a liquid crystal has been put to practical use in a 20-inch or more large-screen that is typified by liquid crystal display TV. In recent years, a liquid crystal display device integrated with driving circuit that comprises TFT in which a polycrystalline silicon film is used as an active layer is realized.

15           However, there is a problem that the TFT using a polycrystalline silicon film result in lower withstanding pressure of drain junction. It resulted that junction leak current (hereinafter, OFF-leak current) is increased. It is known that a lightly doped region (LDD) is effective for reducing the OFF-leak current.

          The problem is pointed out that high electric field is generated at the vicinity of  
20   the drain region, then, hot carriers are trapped by a gate insulating film on the LDD region, and then, a device characteristic such as threshold value is greatly deteriorated. The TFT in which the gate electrode is overlapped with the LDD region to prevent the deterioration of hot carriers is disclosed in JP 2001-294787. The gate overlapped LDD structure TFT has higher current driving ability compared to the normal LDD structure TFT, and  
25   suppresses the deterioration due to hot carriers by easing effectively the high electric field at the vicinity of the drain region.

          However, according to the gate overlapped LDD structure TFT disclosed in above publication, an impurity region for forming an LDD region is formed on the semiconductor layer, then, the gate electrode is formed thereon to overlap with the LDD  
30   region. The manufacturing method cannot regulate accurately the portion that is

overlapping with the gate electrode along with the miniaturization of design rule.

On the other hand, the preferred example of manufacturing the gate overlapping LDD structure TFT in a self-aligning manner is disclosed in JP2002-14337. The technique disclosed in the publication is that at least two layered conductive layer is  
5 subjected to once exposure and plural etching, then, the upper layer and the lower layer are formed to have different thickness and shape, and then, an ion doping is conducted thereon. Consequently, an LDD region that is overlapped with a gate electrode can be formed in a self-aligning manner.

Of course, it is necessary that the LDD length (the length for channel length) is  
10 optimized depending on the driving voltage of TFT in order to maximize the functions of the LDD overlapped with the gate electrode as a countermeasure against deteriorations due to hot carriers. That is, there is optimum length for easing effectively the high electric field region in the vicinity of the drain region.

The technique disclosed in above-mentioned publication has two steps: in the  
15 first step, two laminated conductive layers are subjected to etching to have a taper shape, in the second step, only the upper layer of the laminated conductive layers in the taper shape is selectively subjected to anisotropic etching, and can regulate LDD length by controlling the taper angle.

## 20 SUMMARY OF THE INVENTION

In order to etch not only the gate electrode but also an edge portion or a side wall portion of a film in accordance with mask pattern, the etching is performed with trimming the width of a mask pattern by dry etching. For that purpose, the selection of kinds of gas for etching, the regulation of bias voltage, and the selection ratio of materials of mask  
25 pattern and film are important matters.

In the conventional technique using the gate electrode having at least two layers laminated structure, it is necessary that a taper angle (an angle with the substrate surface) is decreased during processing steps of the gate electrode in order to regulate LDD length. For that purpose, the mask pattern must be largely trimmed. The mask pattern should  
30 leave a margin for thickness since it will be trimmed. It results in a problem that a

microscopic mask pattern cannot be formed.

With respect to an issue concerning selective ratio of etching processing, the relationship between etching gas and the subject needs to be considered. An area of display device, the problem of signal delay should be solved along with growing in size of screen. It is necessary to use materials having low resistivity typified by aluminum. Specifically, sheet resistance needs at most  $0.2 \Omega/\square$  in consideration of approximately 20-inch screen.

In order to drive a TFT having channel portion  $10 \mu\text{m}$  in length at 10 to 20 V, LDD region needs at least  $1 \mu\text{m}$  (preferably,  $1.5 \mu\text{m}$ ) in length (length of overlapping portion with the gate electrode). In this case, it is necessary to form approximately  $20^\circ$  taper angles with aluminum film having  $0.5 \mu\text{m}$  in thickness have according to the above-mentioned conventional technique. However, since aluminum is hard to be subjected to taper processing, such small taper angle cannot be formed by dry etching.

In view of the foregoing, an object of the present invention is to provide a method of manufacturing TFT, through which the flexibility is brought in design of LDD that is overlapping with the gate electrode that is formed in a self-aligning manner, in particular, TFT that is resistant to hot carriers can be formed with repeatability.

The applicant has considered the length of an LDD overlapping with a gate electrode (hereinafter, referred to as  $L_{ov}$  for the sake of convenience), which is necessary for reducing hot-carrier-induced degradation of a thin-film transistor (TFT) as follows.

First, defining the time until the maximum field-effect mobility decreases by 10 % as lifetime when the  $L_{ov}$  relative to the degradation of a TFT is a predetermined value, voltages at which the lifetime becomes ten years are derived as ten-year guaranteed voltages from a linear relationship obtained by plotting the reciprocal of a drain voltage on a semilogarithmic graph, as shown in Fig. 11. For example, in Fig. 11, the ten-year guaranteed voltage of a TFT with a length  $L_{ov}$  of  $1.0 \mu\text{m}$  is 16 V. Fig. 12 is the plot of the values of the estimated guaranteed voltages thus obtained when the  $L_{ov}$  is  $0.5 \mu\text{m}$ ,  $0.78 \mu\text{m}$ ,  $1.0 \mu\text{m}$ ,  $1.5 \mu\text{m}$ , and  $1.7 \mu\text{m}$ . Fig. 12 also shows drain voltages as 20-hour guaranteed voltages, at which the time until the ON-state current of the TFT changes by 10 % is 20 hours in a bias stress test.

The hot-carrier-induced degradation is insignificant with low driving voltage, however, it becomes non-negligible with a driving voltage of 10 V or more. Fig. 12 clearly shows that when the driving voltage is 16 V, the Lov must be 1  $\mu\text{m}$ , and preferably, 1.5  $\mu\text{m}$  or more.

5 In order to satisfy the above requirements, the present invention provides a process for producing a semiconductor device by which an LDD overlapping with a gate electrode is formed by self alignment, wherein a gate electrode is formed of a laminate structure comprising a plurality of conductive layers, which is shaped such that the width along the channel length of a lower first conductive layer is larger than that of a second  
10 conductive layer, and the gate electrode is used as a mask during ion doping for forming an LDD. At that time, a mask pattern for forming the gate electrode is processed into an optimum shape, in combination with dry etching in order that the LDD overlapping with the gate electrode (Lov) is 1  $\mu\text{m}$  or more, and preferably, 1.5  $\mu\text{m}$  or more.

A process according to the invention comprises the steps of: forming a laminate  
15 structure comprising a lower first conductive layer and an upper second conductive layer over a semiconductor layer with a gate insulating film interposed therebetween; forming a mask pattern on the laminate structure; forming a first conductive layer pattern having a tapered edge by etching the second conductive layer and the first conductive layer; recessing the edge of the mask pattern remaining on the first conductive layer pattern; and  
20 forming a second conductive layer pattern by selectively etching the second conductive layer in the first conductive layer pattern in accordance with the mask pattern. Accordingly, a second conductive layer pattern is formed in which the width along the channel length of the lower first conductive layer is larger than that of the upper second conductive layer. The projection length of the first conductive layer can be 1  $\mu\text{m}$  or more,  
25 which is used as a mask for shielding ions accelerated by an electric field, so that an LDD region overlapping with the second conductive layer pattern can be formed. In other words, the LDD region can be formed by self alignment. Of course, the second conductive layer pattern can be used as a gate electrode.

In the above arrangement, preferably, the first conductive layer is made of  
30 tungsten, and the second conductive layer is made of aluminum or metal having

aluminum as the main component. Preferably, the edge of the mask pattern is recessed by oxygen plasma treatment.

A process according to the invention comprises the steps of: forming a laminate structure over a semiconductor layer by sequentially depositing a first conductive layer, a  
5 second conductive layer, and a third conductive layer with a gate insulating film interposed therebetween; forming a mask pattern thereon; forming a first conductive layer pattern having a tapered edge; recessing the edge of the mask pattern remaining on the first conductive layer pattern; and forming a second conductive layer pattern by selectively etching the third conductive layer and the second conductive layer in the first  
10 conductive layer pattern in accordance with the mask pattern. Accordingly, a second conductive layer pattern is formed in which the width along the channel length of the lower first conductive layer is larger than that of the upper second conductive layer. The projection length of the first conductive layer can be 1  $\mu\text{m}$  or more, which is used as a mask for shielding ions accelerated by an electric field, so that an LDD region  
15 overlapping with the second conductive layer pattern can be formed. In other words, the LDD region can be formed by self alignment. Of course, the second conductive layer pattern can be used as a gate electrode.

In the above arrangement, preferably, the first conductive layer is made of tungsten, the second conductive layer is made of aluminum or alloy or compound having  
20 aluminum as the main component, and the third conductive layer is made of titanium nitride. Preferably, the edge of the mask pattern is recessed by oxygen plasma treatment.

A process according to the invention comprises the steps of: forming a laminate structure comprising a lower first conductive layer and an upper second conductive layer over a semiconductor layer with a gate insulating film interposed therebetween; forming  
25 a mask pattern thereon; performing plasma treatment for decreasing the taper angle of the edge of the mask pattern; forming a first conductive layer pattern having a tapered edge by etching the second conductive layer and the first conductive layer of the laminate structure by using the mask pattern; forming a second conductive layer pattern by selectively etching the second conductive layer in the first conductive layer pattern.  
30 Accordingly, a second conductive layer pattern is formed in which the width along the

channel length of the lower first conductive layer is larger than that of the upper second conductive layer. The projection length of the first conductive layer can be 1  $\mu\text{m}$  or more, which is used as a mask for shielding ions accelerated by an electric field, so that an LDD region overlapping with the second conductive layer pattern can be formed. In other words, the LDD region can be formed by self alignment. Of course, the second conductive layer pattern can be used as a gate electrode.

In the above arrangement, preferably, the first conductive layer is made of tungsten and the second conductive layer is made of aluminum or metal having aluminum as the main component. Preferably, the edge of the mask pattern is recessed by oxygen plasma treatment.

A process according to the invention comprises the steps of: forming a laminate structure over a semiconductor layer by sequentially depositing a first conductive layer, a second conductive layer, and a third conductive layer with a gate insulating film interposed therebetween; forming a mask pattern thereon; performing plasma treatment for etching the third conductive layer and decreasing the taper angle of the edge of the mask pattern; forming a first conductive layer pattern having a tapered edge by etching the second conductive layer and the first conductive layer of the laminate structure by using the mask pattern; forming a second conductive layer pattern by selectively etching the second conductive layer in the first conductive layer pattern. Accordingly, a second conductive layer pattern is formed in which the width along the channel length of the lower first conductive layer is larger than that of the upper second conductive layer. The projection length of the first conductive layer can be 1  $\mu\text{m}$  or more, which is used as a mask for shielding ions accelerated by an electric field, so that an LDD region overlapping with the second conductive layer pattern can be formed. In other words, the LDD region can be formed by self alignment. Of course, the second conductive layer pattern can be used as a gate electrode.

In the above arrangement, preferably, the first conductive layer is made of tungsten, the second conductive layer is made of aluminum or alloy or compound having aluminum as the main component, and the third conductive layer is made of titanium nitride. Preferably, the width of the mask pattern is decreased by plasma treatment using

a fluorine-based gas.

In the process of forming a gate electrode in a laminate structure comprising a plurality of conductive layers such that the width along the channel length of a first conductive layer is larger than that of a second conductive layer, a step of recessing a mask pattern into a narrow shape is provided between a taper etching process and an anisotropic etching process, so that the length along the channel of the first conductive layer can be 1  $\mu\text{m}$  or more. The use of the gate electrode as a mask during ion doping allows the length of an LDD region overlapping with the gate electrode to be 1  $\mu\text{m}$  or more and increases the lifetime of the TFT against hot-carrier-induced degradation.

The invention can be applied to processes for producing various semiconductor devices comprising MOS transistors formed on a monocrystal semiconductor substrate if only they are transistors having an LDD structure overlapping with a gate electrode.

#### BRIEF DESCRIPTION OF THE DRAWINGS

Figs. 1A to 1E are sectional views for explaining a process for producing a semiconductor device according to the present invention;

Figs. 2A to 2C are sectional views for explaining a process for producing the semiconductor device according to the present invention;

Figs. 3A and 3B are diagrams for explaining a reaction by-product removing effect by taper etching;

Figs. 4A and 4B are diagrams for explaining the effects of a reaction by-product when the taper etching is not performed;

Figs. 5A to 5E are sectional views for explaining another process of producing a semiconductor device according to the present invention;

Fig. 6 is a diagram for explaining the arrangement of an inductively coupled plasma (ICP) etching device;

Fig. 7 is a diagram for explaining the change in the taper angle of a mask pattern;

Fig. 8 is a diagram for explaining the relationship between the recess width  $d$  of a second conductive layer and the length  $L_{ov}$  of a gate overlap TFT;

Fig. 9 is an image through a scanning electron microscope (SEM) showing the



form of a conductive layer pattern that is etched according to a first embodiment;

Fig. 10 is an SEM image showing the form of a conductive layer pattern that is etched according to a second embodiment;

Fig. 11 is a characteristic diagram of estimated lifetime of a TFT in a bias stress  
5 test, plotting Lov dependency;

Fig. 12 is a graph showing the Lov dependency of an estimated guaranteed voltage (10%-deterioration of ON-state voltage);

Fig. 13 is a top view showing the arrangement of active-matrix pixels of the semiconductor device according to the invention; and

10 Fig. 14 is a diagram of an example of the semiconductor device.

### DESCRIPTION OF THE PREFERRED EMBODIMENTS

Embodiments of the present invention will be specifically described hereinafter with reference to the drawings. It should be understood that the invention is not limited to  
15 the following embodiments and that various modifications may be made without departing from the spirit and scope thereof. The same elements throughout the following embodiments are given the same reference numerals.

#### [First Embodiment]

20 In this embodiment, a process will be described in which a gate electrode is used as a mask during ion doping, an LDD overlapping with the gate electrode (Lov) is formed by self alignment, and the length of Lov can be 1  $\mu\text{m}$  or more. More specifically, after a first conductive layer pattern has been formed, the edge of a mask pattern remaining thereon is recessed, and a second conductive layer in the first conductive layer pattern is  
25 in turn selectively etched to form a second conductive layer pattern in accordance with the mask pattern.

Referring to Fig. 1A, a first insulating film (base film) 101, a semiconductor layer 102, and a second insulating film (gate insulating film) 103 are formed on a glass substrate 100, on which a first conductive layer 104, a second conductive layer 105, and a  
30 third conductive layer 106 are formed. A mask pattern 107 is formed of a photoresist by

photolithographic processing.

The first conductive layer 104 is formed of high-melting metal with a thickness of 30 to 50 nm, such as tungsten (W), chromium (Cr), tantalum (Ta), titanium (Ti), and molybdenum (Mo). The second conductive layer 105 is formed of aluminum or alloy or  
5 compound having aluminum as the main component (typically, alloy or compound having aluminum and 0.1-5 wt % of one or a plurality of components selected from the group of titanium, silicon, scandium, and niobium) in a thickness of 300 to 600 nm. This is for the purpose of increasing the heat stability of aluminum to prevent the occurrence of aluminum spike.

10 The third conductive layer 106 is formed of high-melting metal such as tungsten (W), chromium (Cr), and titanium (Ti) or their nitride. The third conductive layer 106 is provided to improve the heat resistance of the laminate structure having aluminum as the main component and is not the essential component for the invention. Combination with tungsten used as the first conductive layer facilitates selective processing, since titanium  
15 nitride can be processed with the same etching gas as that for aluminum.

Referring next to Fig. 1B, the second conductive layer 105 and the third conductive layer 106 are etched by dry etching. A mixture of boron trichloride ( $\text{BCl}_3$ ), chloride ( $\text{Cl}_2$ ), and carbon tetrafluoride ( $\text{CF}_4$ ) is used as etching gas. To increase etching rate, a dry etching device that uses a high-density plasma source such as electron  
20 cyclotron resonance (ECR) or inductively coupled plasma (ICP). In order to process the edge or the sidewall in a tapered shape in accordance with the mask pattern, a negative bias voltage is applied to the substrate side.

The photoresist mask pattern 107 is sputtered by ions accelerated by an electric field, so that a reaction by-product is adhered to the sidewall of the workpiece. This is  
25 also called a sidewall protective film. The reason why the second conductive layer 105 having aluminum as the main component is tapered in this process step is to remove the sidewall protective film. More specifically, when the tapered second conductive layer 105 is etched anisotropically thereafter, as shown in Fig. 3A, the reaction by-product is hardly deposited on the sidewall, so that it can be etched without a residue to form the  
30 pattern of a second conductive layer 105', as shown in Fig. 3B. On the other hand, when

the sidewall of the second conductive layer 105 is substantially vertical, as shown in Fig. 4A, a reaction by-product is deposited during etching, therefore, when it is etched anisotropically thereafter, the reaction by-product remains to cause malformation, as shown in Fig. 4B. In other words, when at least the second conductive layer 105 is tapered in this process step, the sidewall protective film can be removed.

Referring then to Fig. 1C, the etching gas is changed to a mixture of  $\text{CF}_4$ ,  $\text{Cl}_2$ , and oxygen ( $\text{O}_2$ ) to etch tungsten that is the first conductive layer 104. Of course, although all the conductive layers may be etched at the same time, the etching time for the thick second conductive layer 105 must be set longer in consideration of the variations in etching rate. In such a case, when the base film is made of silicon oxide, it is etched to become extremely thin. Therefore, in order to prevent it, the two-stage etching is performed.

In this way, a first conductive layer pattern 108 formed of a first conductive layer 104', the second conductive layer 105', and a third conductive layer 106' is formed on the second insulating film 103, as shown in Fig. 1C. The angle formed by the tapered edge of the first conductive layer pattern 108 and the substrate 100 is set to 10 to 20 degrees. The angle is determined mainly depending on the relationship with the film thickness of the second conductive layer 105', however, the length of the tapered section is set to about 0.5 to 1.5  $\mu\text{m}$ .

Thereafter, the edge of the photoresist mask pattern 107 is recessed by oxygen plasma treatment. The photoresist serving as the member of the mask pattern 107 is etched by the oxygen plasma treatment to be reduced entirely. The recess width of the pattern can freely be set depending on the treatment time. The length of  $L_{ov}$  can be substantially determined depending on the recess width (refer to Fig. 1D).

The second conductive layer 105' and the third conductive layer 106' are selectively etched in accordance with a mask pattern 107' using a mixture of  $\text{BCl}_3$  and  $\text{Cl}_2$  as etching gas. In this case, the bias voltage to be applied to the substrate side is decreased to thereby leave the first conductive layer 104'. The edge of the second conductive layer 105' is recessed inward from the first conductive layer 104', and the length of  $L_{ov}$  is determined depending on the recess width, as will be described later. In

this manner, a second conductive layer pattern 109 formed of the first conductive layer 104', a second conductive layer 105'', and a third conductive layer 106'' is formed, which acts as a gate electrode at a part intersecting with the semiconductor layer 102 (refer to Fig. 1E).

5           The addition of one-conduction type impurity to the second insulating film 103, that is, the formation of an LDD or a source/drain region can be performed by self alignment using the second conductive layer pattern 109. Fig. 2A shows a doping process for forming an LDD that overlaps with the gate electrode, wherein ions of the one-conduction type impurity are passed through the first conductive layer 104' and are  
10 added to the semiconductor layer 102 thereunder to form a first-concentration one-conduction type impurity region 110. In this case, an acceleration voltage of 50 kV or more is required depending on the film thickness of the second insulating film 103 and the first conductive layer 104'. The concentration of the impurity in the first-concentration one-conduction type impurity region 110 is set at  $1 \times 10^{16}$  to  $5 \times$   
15  $10^{18}/\text{cm}^3$  (peak value) in the case of the LDD.

In the doping process for forming a source/drain region, the second conductive layer pattern 109 is used as a mask for shielding ions and a second-concentration one-conduction type impurity region 111 is formed on the outside of the first-concentration one-conduction type impurity region 110. In such a case, the  
20 acceleration voltage is set at 30 kV or less. The concentration of the impurity in the second-concentration one-conduction type impurity region 111 is set at  $1 \times 10^{19}$  to  $5 \times 10^{21}/\text{cm}^3$  (peak value).

Then, a third insulating film 112 made of silicon nitride, a fourth insulating film 113 made of a low-dielectric organic compound material, and a wire 114 are formed.

25           As described above, according to the embodiment, a TFT that has an LDD overlapping with a gate electrode (Lov) and having a length of 1  $\mu\text{m}$  or more can be formed by self alignment using the gate electrode as a mask during ion doping. Since the length of the LDD region overlapping with the gate electrode is 1  $\mu\text{m}$  or more, the lifetime of the TFT can be increased against hot-carrier-induced deterioration.

30

[Second Embodiment]

In this embodiment, a process will be described in which a gate electrode is used as a mask during ion doping, an LDD overlapping with the gate electrode (Lov) is formed by self alignment, and its length can be 1  $\mu\text{m}$  or more. More specifically, a mask pattern  
5 is formed on a laminate structure for forming a gate electrode, the mask pattern is subjected to plasma treatment to decrease the taper angle of the edge thereof, the laminate structure is etched using the mask pattern to form a first conductive layer pattern having a tapered edge, and a second conductive layer in the first conductive layer pattern is selectively etched to form a second conductive layer pattern.

10 First, as in the first embodiment of Fig. 1A, the first insulating film 101, the semiconductor layer 102, the second insulating film 103, the first conductive layer 104, the second conductive layer 105, the third conductive layer 106, and the mask pattern 107 are formed on the substrate 100 (refer to Fig. 5A).

Next, the taper angle at the edge of the mask pattern 107 is decreased by plasma  
15 treatment. At the same time, the third conductive layer 106 is reduced. An applicable etching gas is a fluorine-based gas, such as sulfur hexafluoride ( $\text{SF}_6$ ) and nitrogen trifluoride ( $\text{NF}_3$ ).

The taper angle is an angle formed by the surface of the substrate 100 and the sidewall of the mask pattern 107, or an angle formed by the mask pattern 107 and the  
20 surface of the layer thereunder. A taper angle  $\alpha_2$  after the plasma treatment can be decreased relative to a taper angle  $\alpha_1$  in the initial state of the mask pattern 107. More specifically, the resist is etched by the fluorine-based gas, so that the edge is recessed and also the taper angle is decreased. At that time, the mask pattern 107 is preferably tapered to a certain extent rather than rectangular in initial cross section, because the amount of  
25 recess can be increases. Fig. 5B shows the mask pattern 107' and the third conductive layer 106' after the plasma treatment.

Then, referring to Fig. 5C, the second conductive layer 105 and the third conductive layer 106' are etched by dry etching. A mixture of  $\text{BCl}_3$ ,  $\text{Cl}_2$ , and  $\text{CF}_4$  are used as etching gas. In order to process the edge or the sidewall into tapered shape in  
30 accordance with the mask pattern 107', a negative bias voltage is applied to the substrate

side. Decreasing the taper angle of the edge of the mask pattern 107' in the previous process step increases the amount of the recess of the mask pattern 107' and to decrease the taper angle of the sidewall of the second conductive layer 105 to be etched by the etching process.

5           Then, referring to Fig. 5D, the etching gas is changed to  $\text{CF}_4$ ,  $\text{Cl}_2$ , and  $\text{O}_2$  to etch tungsten that is the first conductive layer 104. In this way, the first conductive layer pattern 108 formed of the first conductive layer 104', the second conductive layer 105', and the third conductive layer 106' is formed on the second insulating film 103. The angle formed by the tapered edge of the first conductive layer pattern 108 and the surface  
10 of the substrate 100 is set to 10 to 20 degrees. The angle is determined mainly depending on the relationship with the film thickness of the second conductive layer 105', the length of the tapered section is set to about 0.5 to 1  $\mu\text{m}$ .

          The second conductive layer 105' and the third conductive layer 106' are selectively etched in accordance with the mask pattern 107' using  $\text{BCl}_3$  and  $\text{Cl}_2$  as etching  
15 gas. In this case, the bias voltage to be applied to the substrate side is decreased to thereby leave the first conductive layer 104'. The edge of the second conductive layer 105' is recessed inward from the first conductive layer 104', and the length of  $L_{ov}$  is determined depending on the recess width, as will be described later. In this manner, the second conductive layer pattern 109 formed of the first conductive layer 104', the second  
20 conductive layer 105'', and the third conductive layer 106''' is formed, which acts as a gate electrode at a part intersecting with the semiconductor layer 102 (refer to Fig. 5E).

          Hereinafter, according to the procedure shown in Figs. 2A to 2C, as in the first embodiment, an LDD overlapping with the gate electrode ( $L_{ov}$ ) is formed by self alignment, and a TFT having an  $L_{ov}$  length of 1  $\mu\text{m}$  or more is formed. Thus, since the  
25 length of the LDD region overlapping with the gate electrode can be 1  $\mu\text{m}$  or more, the lifetime of the TFT can be increased against hot-carrier-induced degradation.

#### [Examples]

##### [Example 1]

30           An example of forming a gate electrode according to the procedure of the first

embodiment will be described. The present example will be discussed with reference to Figs. 1A to 1E.

First, the first insulating film 101 is formed of a silicon oxynitride film of 150 nm in thickness on the aluminosilicate-glass substrate by plasma chemical-vapor deposition (CVD). The semiconductor layer 102 is made of a crystalline silicon film formed by crystallizing an amorphous silicon film of 50 nm in thickness by laser annealing so as to be separated into the form of an island. The second insulating film 103 is formed of a silicon oxynitride film of 115 nm in thickness using monosilane ( $\text{SiH}_4$ ) and dinitrogen oxide ( $\text{N}_2\text{O}$ ) as source gas by plasma CVD. The first conductive layer 104 made of tungsten is formed in a thickness of 30 nm, the second conductive layer 105 made of aluminum that contains silicon is formed in a thickness of 500 nm, and the third conductive layer 106 made of titanium nitride is formed in a thickness of 20 nm. The mask pattern 107 is made of a positive photoresist in a thickness of 1.5  $\mu\text{m}$ . The width of the mask pattern 107 may be set as appropriate, however, in this example, photolithographic processing is performed using mask patterns with widths of 4.5  $\mu\text{m}$  and 10  $\mu\text{m}$  (refer to Fig. 1A).

Next, the second conductive layer (aluminum that contains silicon) 105 and the third conductive layer (titanium nitride) 106 are etched by dry etching. For etching, an ICP etching device is used. Fig. 6 shows the arrangement of the ICP etching device. A gas supply unit 803 for etching and an exhaust unit 804 for maintaining a reaction chamber 801 under reduced pressure are connected to the reaction chamber 801. A plasma generation unit comprises a spiral coil 802 for inductively coupling to the reaction chamber 801 through a quartz plate and a radiofrequency (13.56 MHz) power supply unit 805. A bias voltage is applied to the substrate side by a radiofrequency (13.56 MHz) power supply unit 806 to cause self-bias on a stage 807 having the substrate thereon. Main parameters for etching process are the type of etching gas to be supplied, radiofrequency power supplied by the radiofrequency (13.56 MHz) power supply units 806 and 807, and etching pressure.

Referring to Fig. 1B, a mixture of  $\text{BCl}_3$ ,  $\text{Cl}_2$ , and  $\text{CF}_4$  is used as etching gas. The etching pressure is set at 0.7 Pa and 800 W of power for generating plasma and 500 W of

power for biasing the substrate are supplied. Referring then to Fig. 1C, the etching gas is changed to CF<sub>4</sub>, Cl<sub>2</sub>, and O<sub>2</sub> to etch tungsten that is the first conductive layer 104. The conditions for the etching are 1.0 Pa of etching pressure, and 500 W of power for generating plasma, and 20 W of power for biasing the substrate. In this way, the first  
 5 conductive layer pattern 108 can be formed.

The edge of the photoresist mask pattern 107 is then recessed by oxygen plasma treatment. In the oxygen plasma treatment, the ICP etching device is used similarly, wherein 80 sccm of O<sub>2</sub> is supplied, and 450 W of power for generating plasma and 100 W of power for biasing the substrate are supplied under a treatment pressure of 1.2 Pa for 30  
 10 sec. The photoresist mask pattern 107 formed by the oxygen plasma treatment is reduced in width and film thickness (refer to Fig. 1D)

Subsequently, anisotropic etching is performed using a mixture of BCl<sub>3</sub> and Cl<sub>2</sub> as etching gas to mainly process the second conductive layer 105'. At that time, 500W of power for generating plasma and 100 W of power for biasing the substrate are supplied  
 15 under an etching pressure of 1.2 Pa. The edge of the second conductive layer 105' is recessed inward from the first conductive layer 104'. In this way, the second conductive layer pattern 109 is formed, which acts as a gate electrode at a portion intersecting with the semiconductor layer 102. The recess width from the edge of the first conductive layer 104' can be 1 to 2 μm. Referring to Fig. 8, the recess width d determines the length Lov.  
 20 Table 1 shows a comparison of the recess widths d depending on whether or not the oxygen plasma treatment has been performed in a process similar to that of this embodiment.

[Table 1]

Pattern width of mask	unit: μm	
	Oxygen plasma treatment performed	Oxygen plasma treatment not performed
4.5	1.288	0.573
10.0	1.713	0.743

25

As clearly shown in Table 1, when the oxygen plasma treatment was performed,



the recess width  $d$  becomes 1.2 to 1.7  $\mu\text{m}$ , depending on the pattern width of the mask, on the other hand, when the oxygen plasma treatment was not performed, the recess width  $d$  is as small as 0.5 to 0.7  $\mu\text{m}$ .

Fig. 9 shows an image through a scanning electron microscope (SEM) showing a typical form when the oxygen plasma treatment has been applied, which shows a state in which a tungsten layer, an aluminum layer, and a resist mask are deposited from below. Said diagram shows an SEM image observed from an oblique direction, and the recess width of the aluminum layer or the projection width of the tungsten layer is estimated to be about 1.5  $\mu\text{m}$ .

In the last stage of the etching process, the thickness of the mask pattern becomes approximately one-tenth of that in the initial stage. The recess width, however, can be freely set in consideration of the film thickness of the resist and the oxygen plasma treatment. In other words, the length  $L_{ov}$  of a TFT having an LDD overlapping with the gate electrode (a gate-overlap TFT) can be freely set.

Thereafter, phosphorous or boron with a concentration of  $1 \times 10^{16}$  to  $5 \times 10^{18}/\text{cm}^3$  (peak value) is added to the first-concentration one-conduction type impurity region 110 comprising the LDD under an acceleration voltage of 50 kV by ion doping. (Refer to Fig. 2A)

In the doping process for forming a source/drain region, the second-concentration one-conduction type impurity region 111 is formed on the outside of the first-concentration one-conduction type impurity region 110 using the second conductive layer pattern 109 as a mask for shielding ions. In such a case, the concentration of phosphorous or boron is set at  $1 \times 10^{19}$  to  $5 \times 10^{21}/\text{cm}^3$  (peak value) under an acceleration voltage of 10 kV. (Refer to Fig. 2B)

After that, hydrogen-containing silicon oxynitride is formed in a thickness of 100 nm by plasma CVD and photosensitive or non-photosensitive acrylic or polyimide resin is formed in a thickness of 1  $\mu\text{m}$ , thereby forming a fourth insulating film 113. Furthermore, the wire 114 is formed as necessary.

In this way, the LDD overlapping with the gate electrode ( $L_{ov}$ ) can be formed by self alignment and also the TFT with an  $L_{ov}$  length of 1  $\mu\text{m}$  or more can be formed.

[Example 2]

An example of producing a gate electrode according to the procedure of the second embodiment will be described. The present example will be discussed with  
5 reference to Figs. 5A to 5E.

First, as in Example 1, the first insulating film 101 formed of a silicon oxynitride film, the semiconductor layer 102 formed of a crystalline silicon film, the second insulating film 103 formed of a silicon oxynitride film, the first conductive layer 104 (tungsten), the second conductive layer 105 (silicon-containing aluminum), the third  
10 conductive layer 106 (titanium nitride), and the mask pattern 107 are formed over the glass substrate 100 (refer to Fig. 5A).

Next, a process for decreasing the taper angle at the edge of the mask pattern 107 is performed by plasma treatment. At the same time, the third conductive layer 106 is reduced.  $\text{SF}_6$  is used for the plasma treatment. 500W of power for generating plasma and  
15 300 W of power for biasing the substrate are supplied under a treatment pressure of 1.9 Pa. The process allows the third conductive layer 106 to be etched, and also the mask pattern 107 to be etched, thereby decreasing in the taper angle of the edge. (Refer to Fig. 5B).

Then, taper etching is performed, aimed at etching of aluminum contained in the second conductive layer 105. A mixture of  $\text{BCl}_3$ ,  $\text{Cl}_2$ , and  $\text{CF}_4$  is used as etching gas.  
20 800W of power for generating plasma and 500 W of power for biasing the substrate are supplied under an etching pressure of 0.7 Pa. (Refer to Fig. 5C).

Then, the etching gas is changed to a mixture of  $\text{CF}_4$ ,  $\text{Cl}_2$ , and  $\text{O}_2$  to etch tungsten that is the first conductive layer 104. The conditions for the etching are an etching pressure of 1.0 Pa, 500W of power for generating plasma, and 20 W of power for biasing  
25 the substrate. In this way, the first conductive layer pattern 108 can be formed. (Refer to Fig. 5D)

Subsequently, anisotropic etching is performed using a mixture of  $\text{BCl}_3$  and  $\text{Cl}_2$  as etching gas to mainly process the second conductive layer 105'. 500 W of power for generating plasma and 100 W of power for biasing the substrate are supplied under an  
30 etching pressure of 1.2 Pa. The edge of the second conductive layer 105' is recessed

inward from the first conductive layer 104'. (Refer to Fig. 5E)

In this way, the second conductive layer pattern 109 is formed, which acts as a gate electrode at a part intersecting with the semiconductor layer 102. The recess width from the edge of the first conductive layer 104' can be set at 1 to 2  $\mu\text{m}$ . Table 2 shows a comparison of the recess widths d depending on whether or not the plasma treatment has been performed in a process similar to that of the embodiment.

[Table 2]

Pattern width of mask	Plasma treatment performed	unit: $\mu\text{m}$
		Plasma treatment not performed
4.5	1.038	0.573
10.0	1.203	0.743

As clearly shown in Table 2, when the plasma treatment was performed, the recess width increases by about 0.45  $\mu\text{m}$  to be 1.0 to 1.2  $\mu\text{m}$ , depending on the pattern width of the mask, on the other hand, when the plasma treatment was not performed, the recess width is as small as 0.5 to 0.7  $\mu\text{m}$ .

Fig. 10 shows an SEM image showing a typical form when the plasma treatment has been applied, showing a laminate structure of a tungsten layer, an aluminum layer, and a resist mask from below. Said diagram shows an SEM image observed from an oblique direction, and the recess width of the aluminum layer or the projection width of the tungsten layer is estimated to be about 1.5  $\mu\text{m}$ .

From then on, the gate overlap TFT can be formed as in Example 1.

### [Example 3]

The invention can apply to semiconductor devices having various display screens. Particularly, the invention is useful for large-screen semiconductor devices whose display screens measure 20 inches or more diagonally.

Fig. 14 is a structural example of a semiconductor device having a display panel 901 mounted in a casing 900, which is applicable to television receivers and monitor

systems of computers. The casing 900 comprises an electronic circuit board 902 and a speaker 903 for sound reproduction, the electronic circuit board 902 incorporating an amplifier, a radiofrequency circuit, and a semiconductor memory and a magnetic memory such as a hard disk acting as memory functions in a semiconductor integrated circuit to  
5 fulfill an image display function.

A display panel 901 can be of a driver-integral type of a combination of an active-matrix pixel circuit 904 in which TFTs are arranged in matrix form using the gate overlap TFTs according to the invention, a scanning-line driving circuit 905, and a data-line driving circuit 906.

10 Fig. 13 is a diagram showing a principal arrangement of the active-matrix pixel circuit 904. A gate electrode 302 intersecting with a semiconductor layer 301 and a data signal line 303 are formed in the same layer. More specifically, it is formed of a laminate structure comprising at least one conductive layer using aluminum as the main component, and the gate electrode and the wiring pattern are formed by the etching  
15 process according to Example 1 or 2. In this manner, the gate overlap TFT with a length  $L_{ov}$  of 1  $\mu\text{m}$  or more can be formed, and the resistance of the data signal line can be decreased. A gate signal line 304 is formed over the upper layer thereof with an interlayer insulating film interposed therebetween and is in contact with the gate electrode 302 through a contact hole. Of course, the wire can be formed of aluminum, thereby  
20 decreasing the resistance of the wire. A wire 305 that connects the data signal line 303 and the semiconductor layer 301 can be formed in the same layer as that of the gate signal line 304. A pixel electrode 306 is made of indium tin oxide (ITO) that is the compound of indium oxide and titanium oxide. The details of such pixels are disclosed in JP2001-313397.

25 The embodiments have taken a semiconductor device as an example. However, the invention is not limited to the embodiments and can be applied to various other semiconductor devices. For example, it can be applied to various fields, in addition to navigation systems, sound-reproducing systems (such as car audio systems and component audio systems), notebook personal computers, game machines, personal  
30 digital assistants (such as mobile computers, cellular telephones, portable game machines,

and electronic books), electrical home appliances such as refrigerators, washing machines, rice cookers, fixed telephones, vacuum cleaners, and clinical thermometers, and railroad wall banners and large-area information displays such as arrival and departure guide plates in railroad stations and airports.

5           Although the embodiments in the invention have been described as above, it is to be understood by those skilled in the art that various changes and modifications may be made without departing from the spirit and scope of the invention.

          As described above, according to the invention, in the process of forming a gate electrode in a laminate structure comprising a plurality of conductive layers such that the  
10   width along the channel length of a first conductive layer is larger than that of a second conductive layer, a step of recessing a mask pattern into a long shape is provided between a taper etching process and an anisotropic etching process, so that the length along the channel of the first conductive layer can be 1  $\mu\text{m}$  or more. The use of the gate electrode as a mask during ion doping allows the length of an LDD region overlapping with the gate  
15   electrode to be 1  $\mu\text{m}$  or more and increases the lifetime of the TFT against hot-carrier-induced degradation.

          According to the invention, a TFT that has an LDD overlapping with a gate electrode (Lov) and having its length of 1  $\mu\text{m}$  or more can be formed by self alignment using the gate electrode as a mask during ion doping. Since the length of the LDD region  
20   overlapping with the gate electrode is 1  $\mu\text{m}$  or more, the lifetime of the TFT can be increased against hot-carrier-induced deterioration.